

TE 4916

U.S. PTO
09/994279



438	Class	Subclass	ISSUE CLASSIFICATION
905			

PATENT NUMBER

5

U.S. UTILITY Patent Application

SCANNED	O.I.P.E. <i>MAH GOA</i>	PATENT DATE
---------	----------------------------	-------------

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/994279	D	438	905	.2812	

APPLICANTS

Tony Chisna
Karl Lauer

TITLE

Method for integrated circuit device and substrate with atomic layer deposition within a single processing chamber

PTO-2040
12/99

Please
Don't remove this coverage -
thanks -

_____	_____
_____	Date Paid
_____	ISSUE BATCH NUMBER
_____ (Date)	_____

prohibited by the United States Code Title 35, Sections 122, 181 and 368.
employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in pocket on right inside flap)